Europäisches Patentamt

**European Patent Office** 

Office européen des brevets



(11) EP 0 820 146 A3

(12)

## **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3: 28.07.1999 Bulletin 1999/30

(43) Date of publication A2: 21.01.1998 Bulletin 1998/04

(21) Application number: 97111053.1

(22) Date of filing: 02.07.1997

(51) Int. Cl.<sup>6</sup>: **H03K 3/356**, H03K 3/0231, H03L 7/099, H03K 5/13, H03K 3/013

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC
NL PT SE

(30) Priority: 16.07.1996 US 682025

(71) Applicant: SEIKO EPSON CORPORATION Tokyo 163 (JP)

(72) Inventors:

 Rogers, Robert Liberty, Missouri 64068 (US)

Chi, Kuang Kai
 San Jose, California 95129 (US)

Chen, Jason C.
 San Jose, California 95129 (US)

 Fujimori, Keitaro Suwa-gun, Nagano (JP)

 Furuya, Yasunari Chino-shi, Nagano (JP)

 Kasahara, Shoichiro Suwa-shi, Nagano (JP)

 Kikuhara, Kazumichi Chino-shi, Nagano (JP)

(74) Representative:
Grünecker, Kinkeldey,
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

## (54) Differential delay element to prevent common mode oscillation and input hysteresis

A system for providing a differential delay element which optimize the prevention of both common mode oscillation and input hysteresis. The system includes a first voltage supply terminal, a second voltage supply terminal and a current-regulating voltage terminal. The system further includes a current-control MOS transistor having its source connected to the first voltage supply terminal and its gate connected to the current-regulating voltage terminal. A pair of inverters are connected to the current-control MOS transistor. Each inverter has an input MOS transistor with its source connected to the drain of the current-control transistor and its gate forming a respective input terminal, and a load MOS transistor with its drain coupled to the drain of the input transistor and forming an output terminal, and its source connected to the second voltage supply terminal. The system still further includes a pair of cross-coupling means to prevent common mode oscillation, each connecting the gate of the load transistor of a respective inverter and the output terminal of the other inverter to form a positive feedback. A pair of MOS diodes are coupled to the load transistors to prevent input hysteresis characteristics. Each diode is coupled between the drain and the source of a respective load

transistor. To prevent both common mode oscillation and input hysteresis, the channel sizes of the diodes substantially equal the channel sizes of the load transistors.

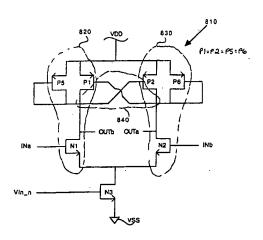


FIG. 8A

EP 0 820 146 A3



## **EUROPEAN SEARCH REPORT**

Application Number EP 97 11 1053

	DOCUMENTS CONSID	ERED TO BE RELEVAN	T	
Category		ndication, where appropriate,	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IntCI.6)
A	US 5 063 311 A (SWA 5 November 1991 * abstract; figures		1,5, 8-10, 18-20	H03K3/356 H03K3/0231 H03L7/099 H03K5/13
A	EP 0 379 955 A (NAT 1 August 1990	SEMICONDUCTOR CORP)	1,5, 8-10, 18-20	H03K3/013
	* abstract; figures	5,4 * .		
P,X	US 5 635 879 A (SUT 3 June 1997 * abstract; figures	TARDJA PANTAS ET AL)	1-20	
P,X	US 5 576 647 A (SUI 19 November 1996 * abstract; figures	FARDJA PANTAS ET AL)	1-20	
				TECHNICAL FIELDS SEARCHED (Int.Cl.6)
				H03K H03L
	The present search report has	been drawn up for all claims		,
	Place of search	Date of completion of the searc		Examiner
	THE HAGUE	8 June 1999		aert, P
X : part Y : part door A : tech	ATEGORY OF CITED DOCUMENTS ioularly relevant if taken alone ioularly relevant if combined with and ument of the same category mological background written disolosure	E : earlier pater after the film ther D : document of L : document of	ited in the application ted for other reasons	ahed on, or

## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 97 11 1053

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

08-06-1999

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5063311	A	05-11-1991	JP	4297117 A	21-10-19
EP 0379955	A	01-08-1990	US CA JP	4876519 A 1303690 A 2233012 A	24-10-19 16-06-19 14-09-19
US 5635879	A	03-06-1997	US WO US	5576647 A 9701216 A 5686867 A	19-11-19 09-01-19 11-11-19
US 5576647	Α	19-11-1996	WO US US	9701216 A 5686867 A 5635879 A	09-01-19 11-11-19 03-06-19
				50358/9 A	03-00-19
			:		
			:		

FORM P0459 o in For more details about this annex : see Official Journal of the European Patent Office, No. 12/82